

Fig. 22

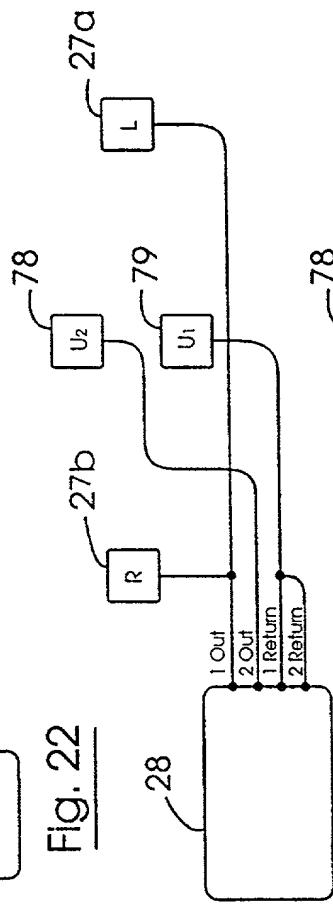


Fig. 23

Diagram illustrating the circuit connections for Fig. 23. The connections are as follows:

- Component **L** is connected to the top terminal of component **U1**.
- Component **U1** is connected to the top terminal of component **U2**.
- Component **U2** is connected to the top terminal of component **R**.
- Component **R** is connected to the top terminal of a central junction point.
- Component **U1** is connected to the bottom terminal of the central junction point.
- Component **U2** is connected to the bottom terminal of the central junction point.
- Component **R** is connected to the bottom terminal of the central junction point.
- The central junction point has four output lines labeled **28**, **27b**, **79**, and **27a** from top to bottom.
- Line **28** connects to the top terminal of a large rectangle.
- Line **27b** connects to the top terminal of component **U1**.
- Line **79** connects to the top terminal of component **U2**.
- Line **27a** connects to the top terminal of component **L**.
- Component **U1** has two return lines labeled **1 Out** and **1 Return** connected to the central junction point.
- Component **U2** has two return lines labeled **2 Out** and **2 Return** connected to the central junction point.

Fig. 24

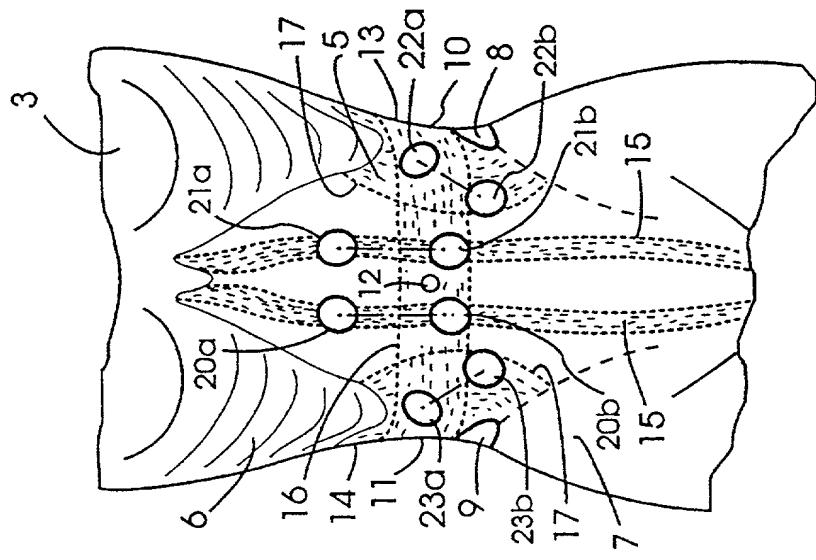
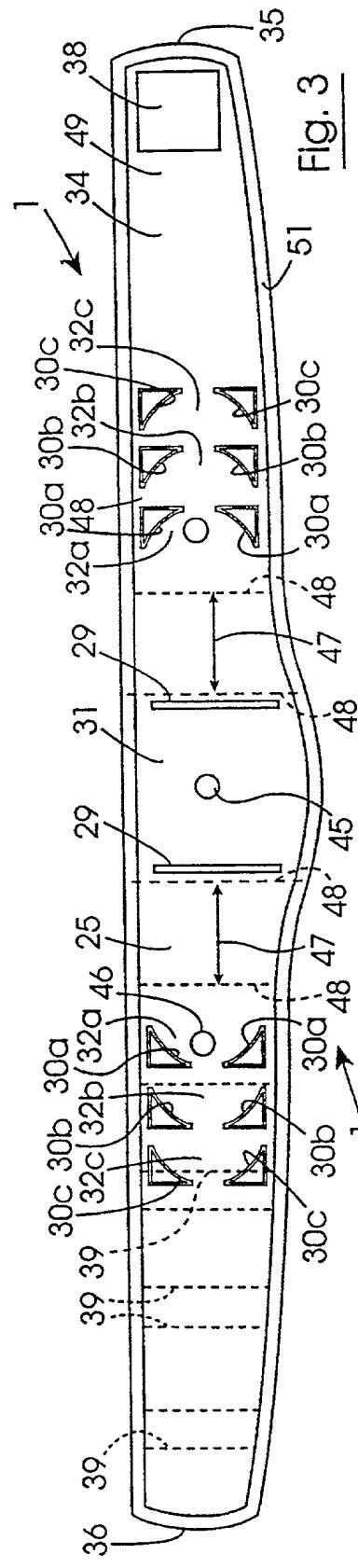


Fig. 1



**SUBSTITUTE SHEET (RULE 26)**

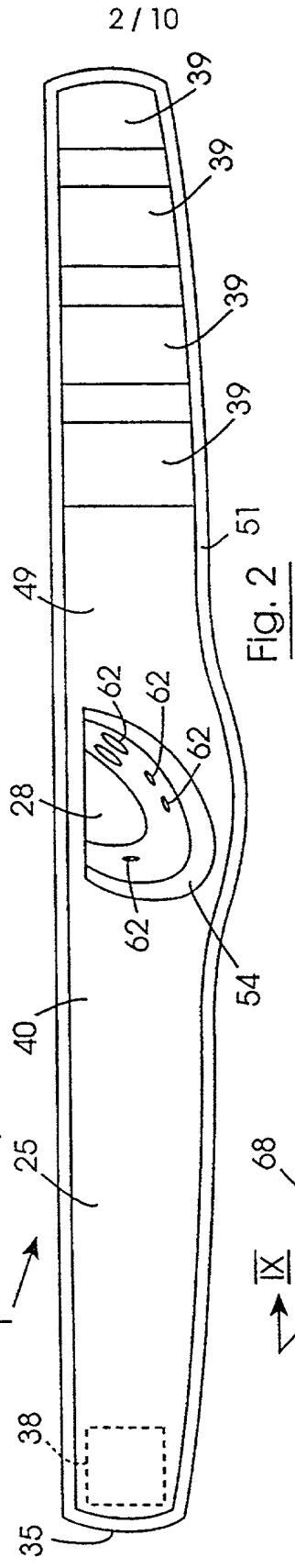


Fig. 2

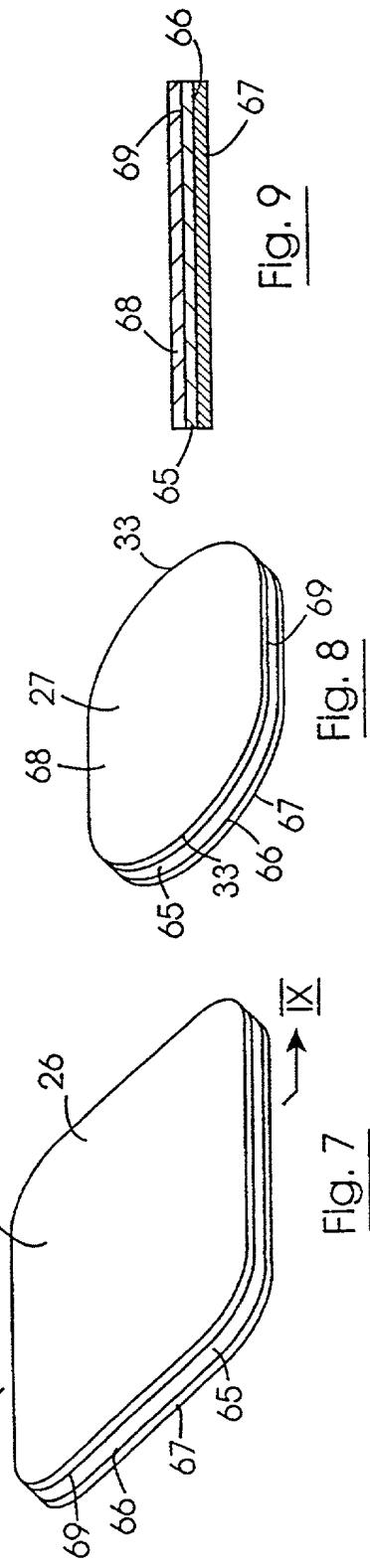


Fig. 9

Fig. 8

Fig. 7

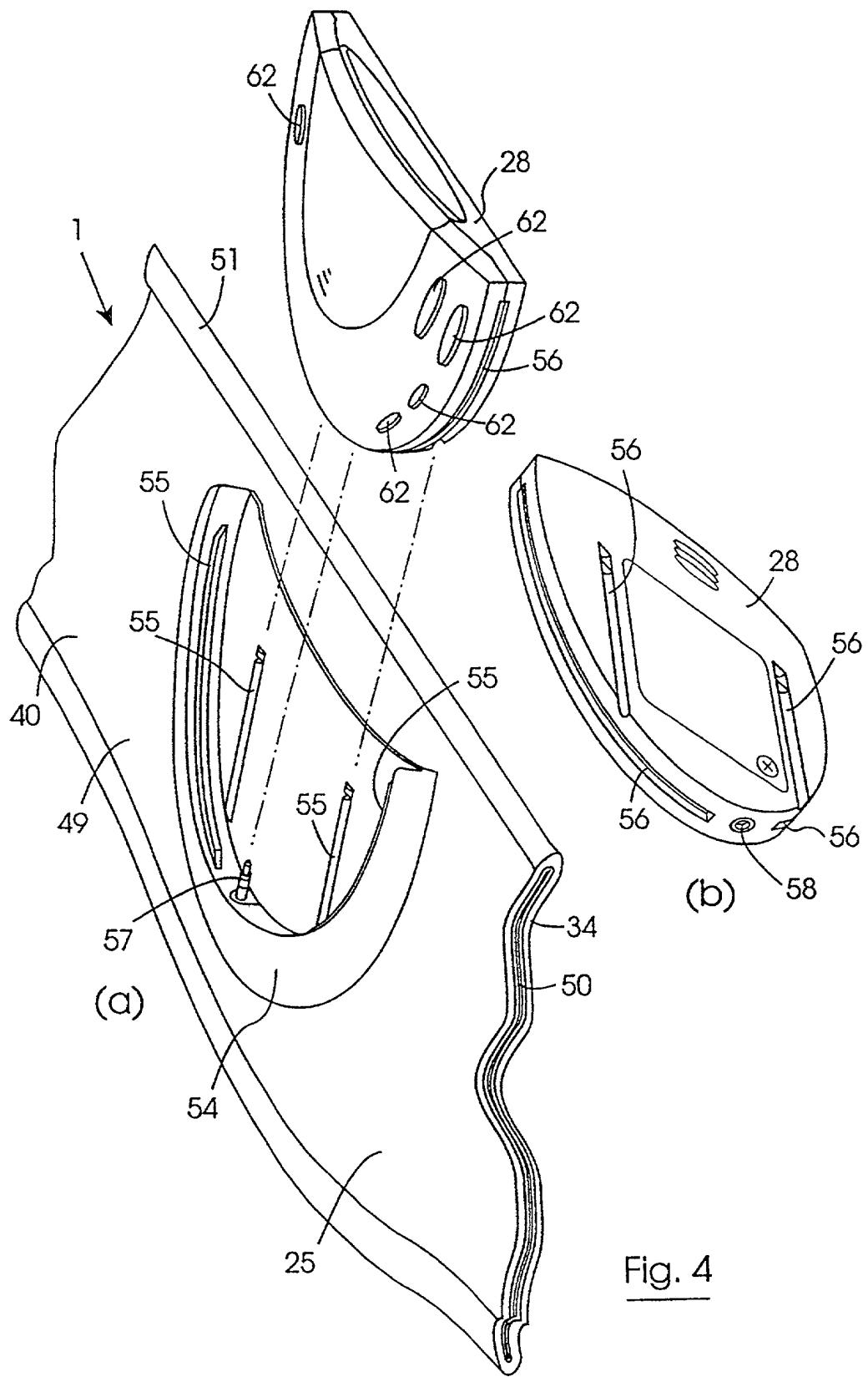


Fig. 4

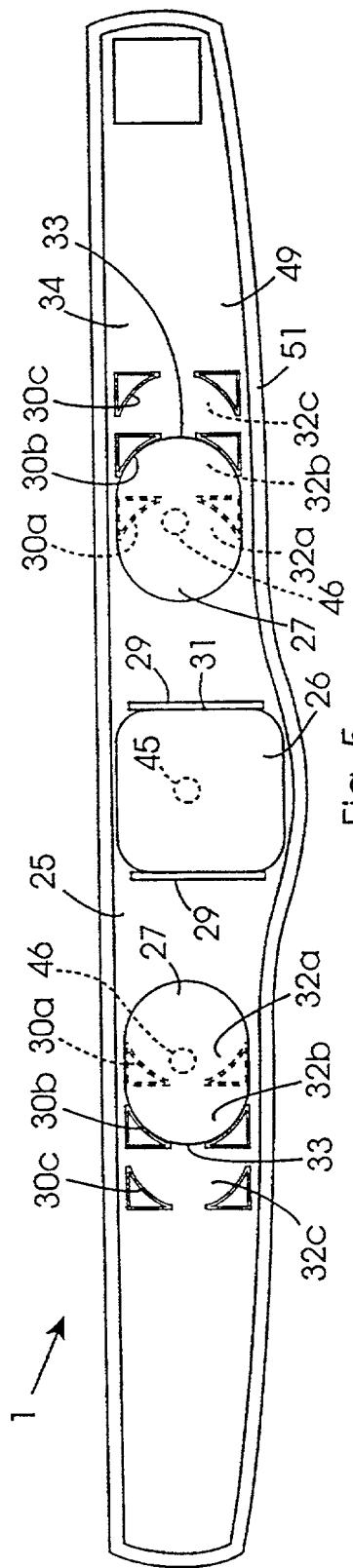


Fig. 5 |

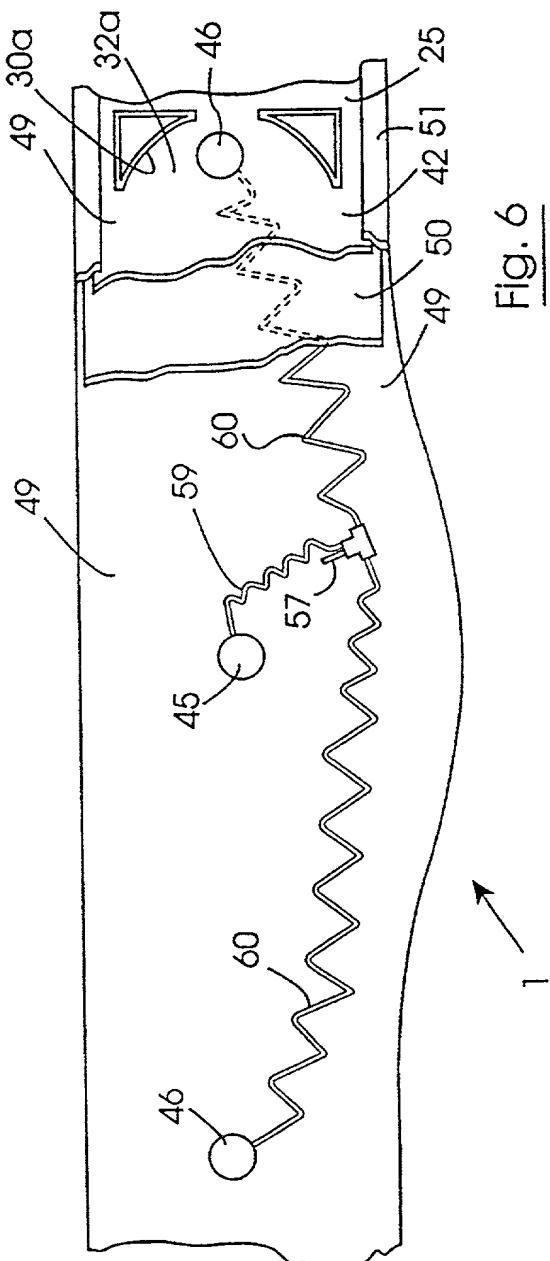


Fig. 6

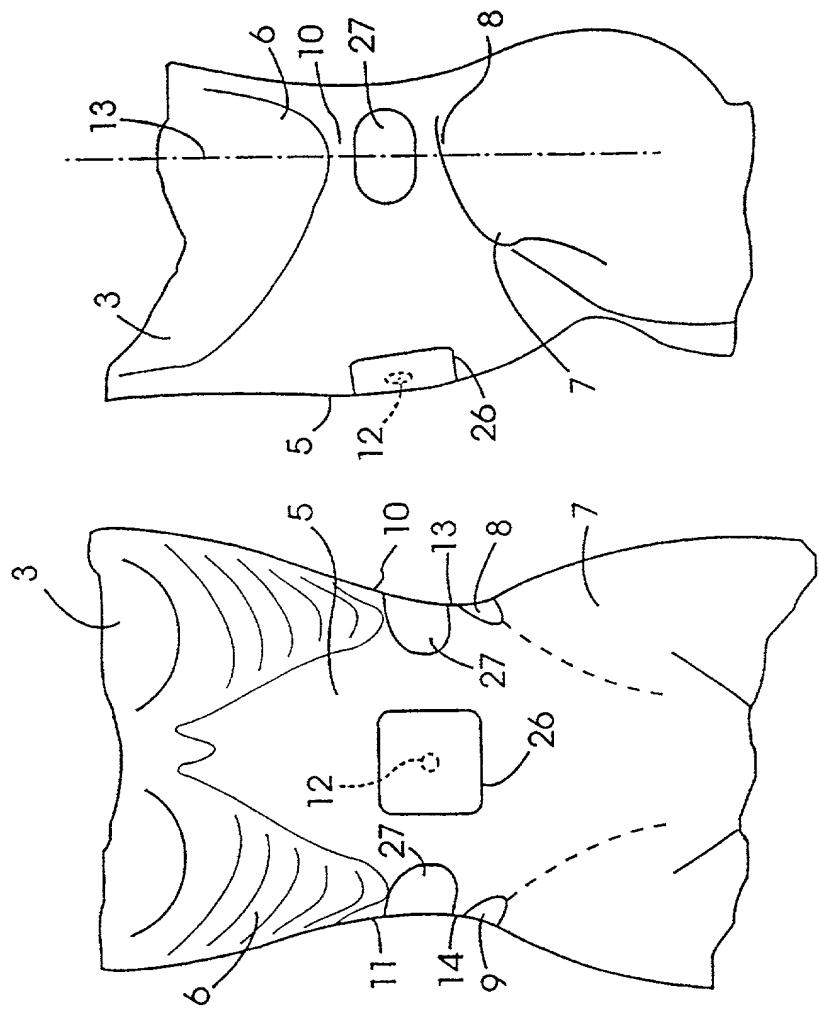


Fig. 12

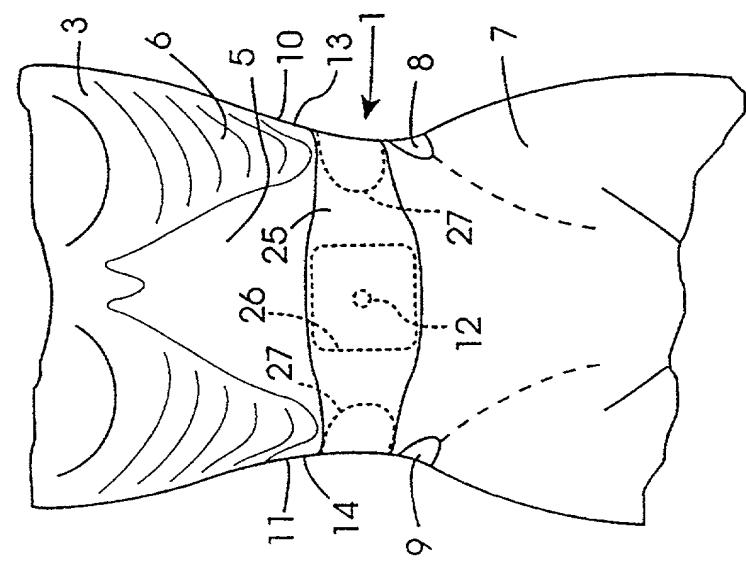


Fig. 10

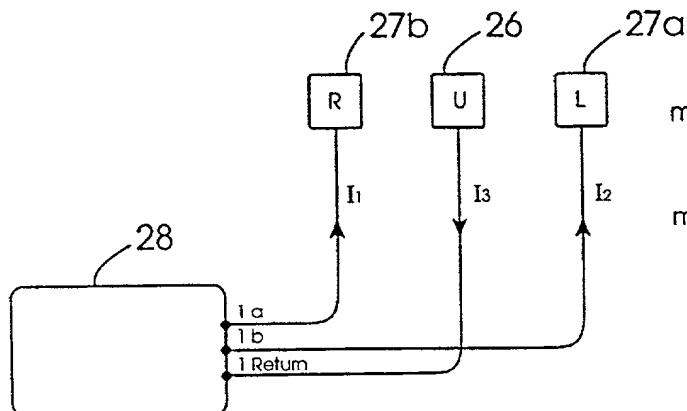


Fig. 13

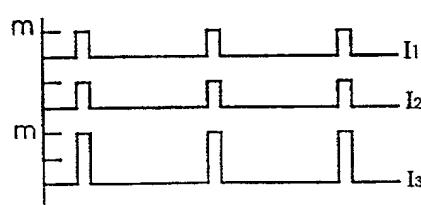


Fig. 14

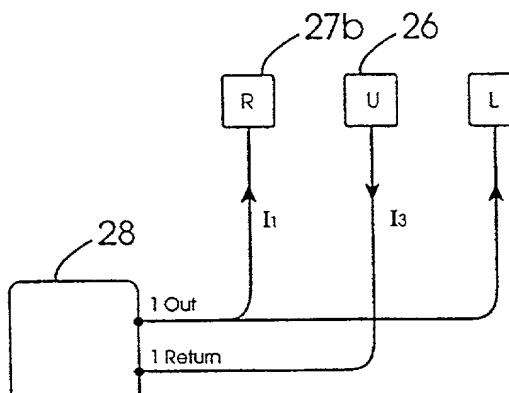


Fig. 15

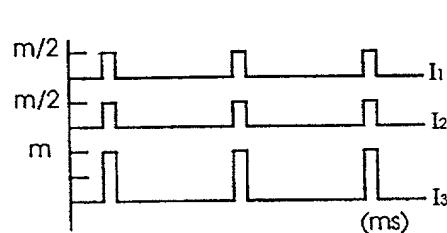


Fig. 16

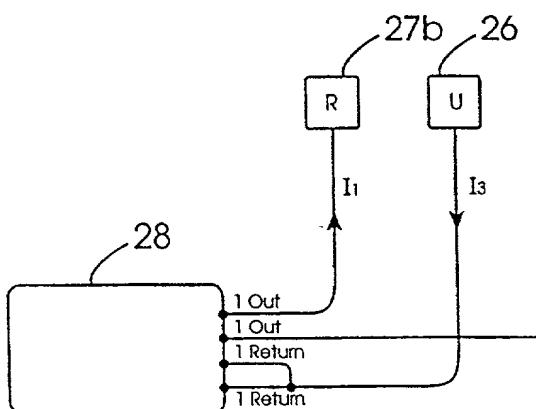


Fig. 17

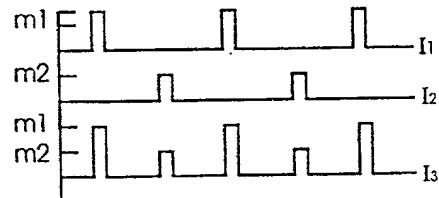


Fig. 18

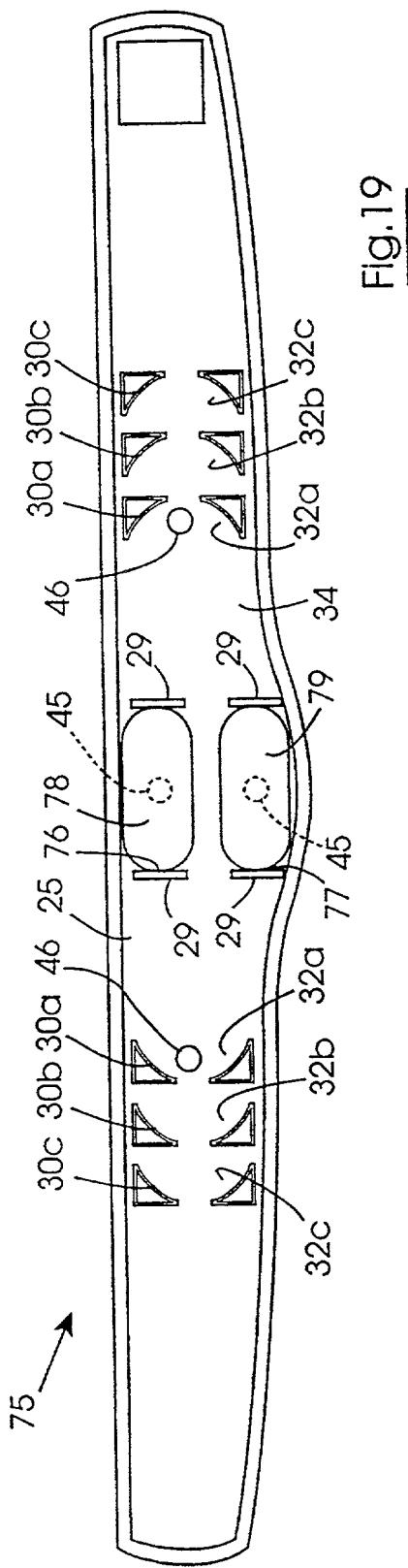


Fig. 19

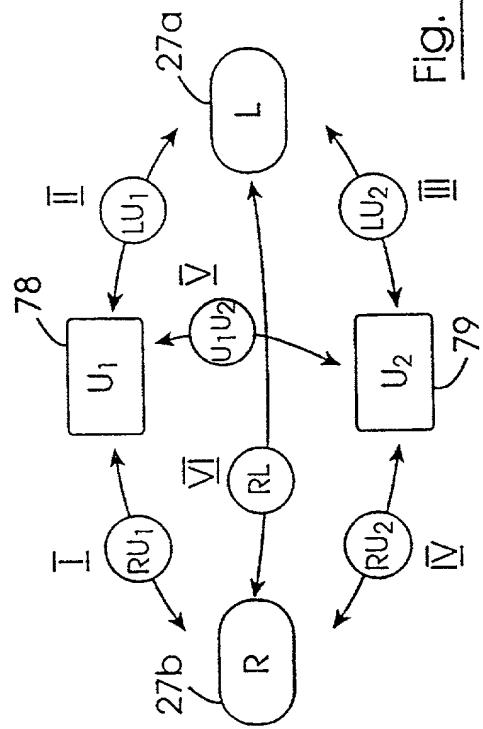


Fig. 25

8 / 10

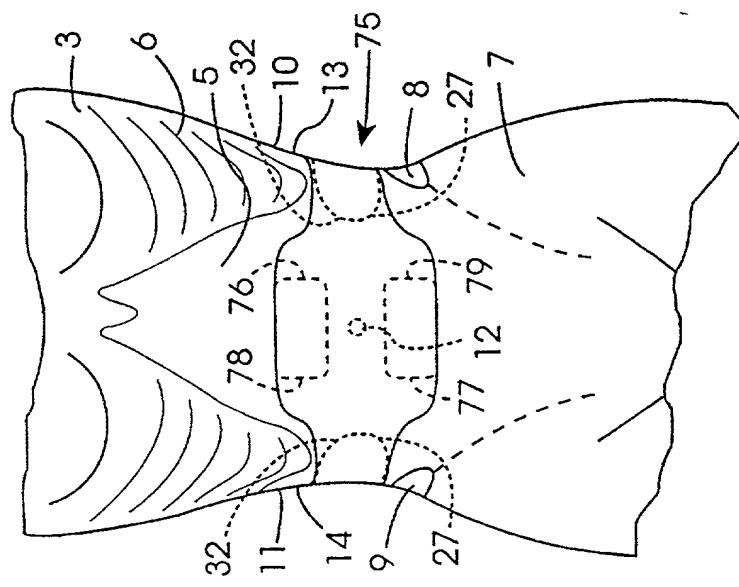


Fig. 20

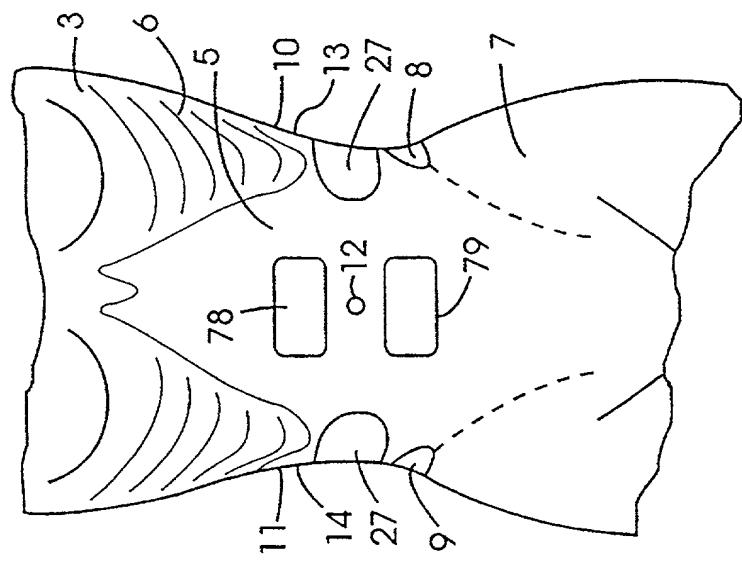


Fig. 21

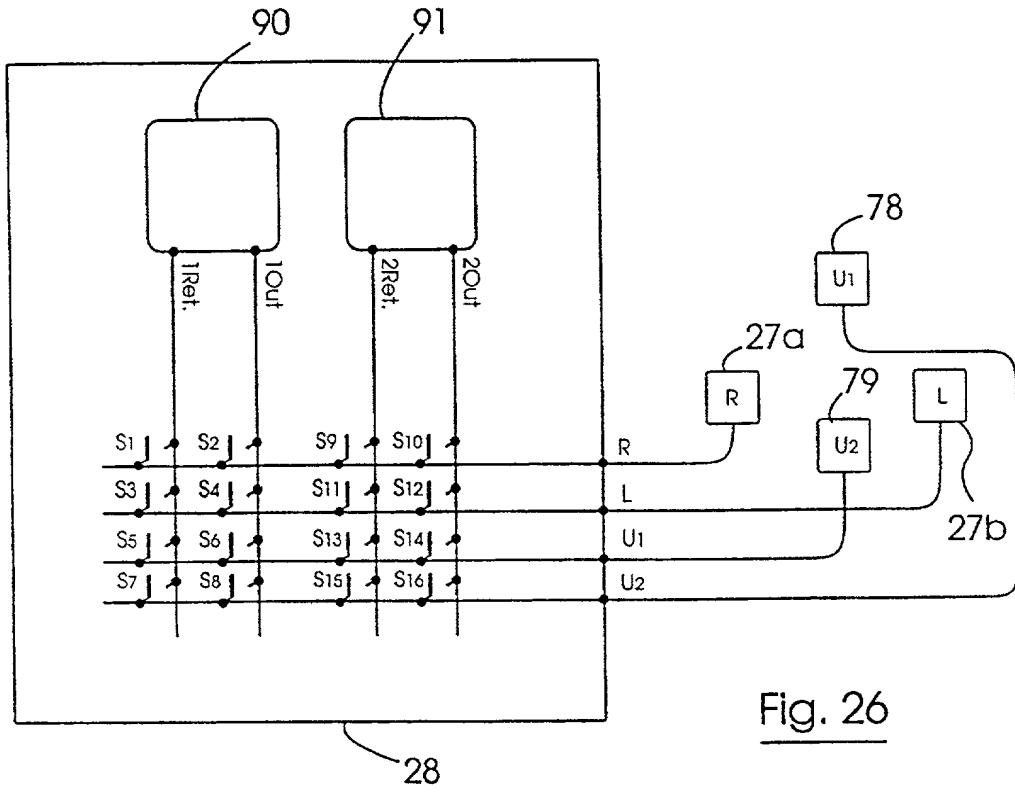


Fig. 26

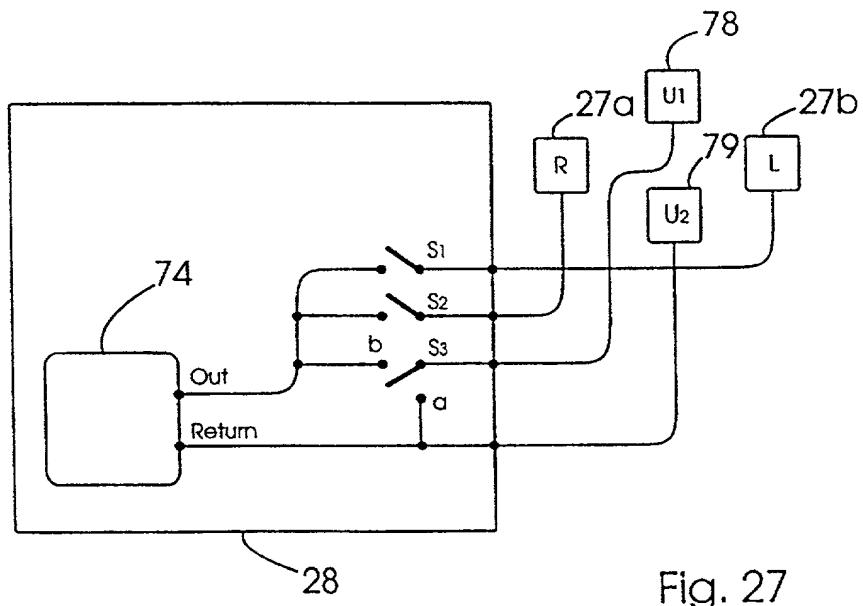


Fig. 27

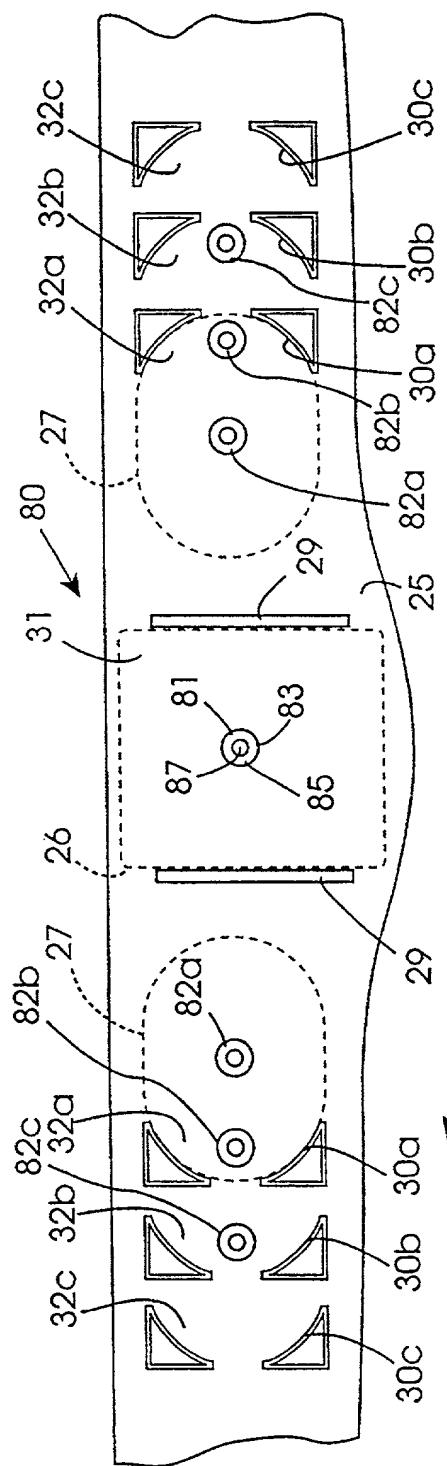


Fig. 28

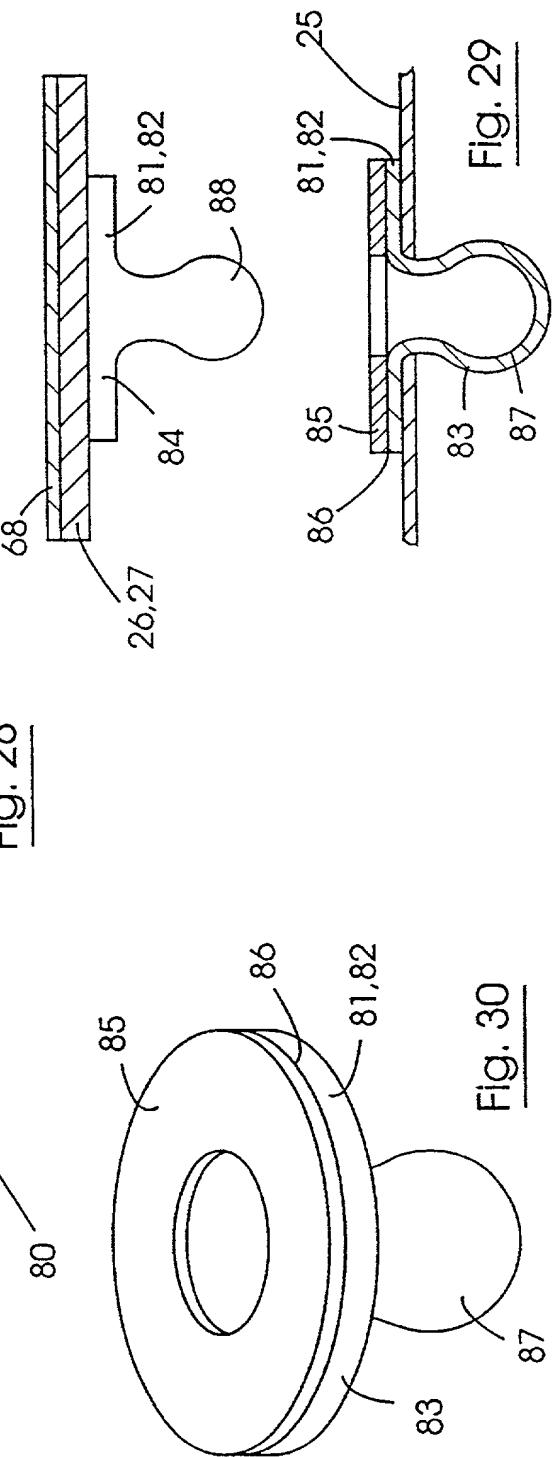


Fig. 29